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A Novel Three-Phase Integrated Inverter for Hybrid Electric Vehicle Applications

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Abstract
Multilevel inverters (MLIs) have become essential in power electronics due to their capability to improve power quality, minimize harmonic distortion, and enhance efficiency in medium and HV applications. It achieves a smoother waveform, reducing total harmonic distortion (THD). Hybrid electric vehicles (HEVs) are increasingly recognized for their ability to reduce fuel consumption and emissions in modern transportation. Their performance largely depends on the efficiency of power conversion systems, particularly in the inverter setup. In this study, a novel 3-phase 25-level MLI configuration is proposed with fewer switches. The primary objective is to reduce harmonics through high-level MLI implementation and motor optimization in electric vehicle applications. Proposed research suggests a novel three-phase 25-level hybrid inverter tailored for hybrid electric vehicles, featuring innovative hybrid DC-DC and DC-AC topologies that utilize fewer switches to enhance cost-effectiveness. Simulation results indicate that the three-phase 25-level MLI improves voltage stability and further mitigates harmonics compared to a single-phase configuration. While comparing with conventional converters, MLIs offer significant benefits, including high-frequency switching and advanced modulation techniques for precise control. It generates output voltage with minimal harmonics, lower dv/dt stress on switches, and introduces common-mode voltage. In particular, the 3-phase 25-level inverter system achieves a smoother waveform, reducing total harmonic distortion (THD). The proposed system has been validated using MATLAB/Simulink. Additionally, the comparative analysis between the proposed 1-ph. and 3-ph. 25-level MLI topologies are also presented.

Keywords: *Hybrid Electric Vehicles (HEV), Multilevel Inverter (MLI), Pulse Width-Modulation (PWM), Phase- Disposition (PD), Total Harmonic Distortion (THD).*

I. INTRODUCTION

Power electronics has emerged as one of the most actively researched and rapidly evolving domains within electrical engineering (Dewi et al., 2022; Koerniawan et al., 2024; Qosidah, 2025). The scope of power electronics continues to expand, especially in solar photovoltaic systems, which are becoming increasingly essential in the modern energy landscape. With the rising demand for uninterrupted, high-quality power and the rapid depletion of non-renewable energy sources, engineers in the field are driven to develop innovative solutions. One significant area of study in power electronics is multilevel inverters (voltage source converters) (Shukla, Goel, and Dhanamjayulu 2026). These inverters have garnered considerable attention for industrial medium-voltage applications.

However, as the number of voltage levels in conventional multilevel inverters (MLIs) increases, the complexity of both the power and control circuits escalates due to the increasing number of

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components (Stöttner et al. 2025) and driving circuits. Additionally, system reliability tends to decrease as the number of discrete elements increases. To enhance efficiency and refine output voltage waveforms, various MLI topologies have been introduced (Faraji and Cha 2025).

Multilevel inverters have become crucial in modern applications, particularly with the increasing integration of renewable energy sources (RES) (Jayaraman et al. 2025). They are widely used in microgrid systems and are particularly advantageous for medium- and high-power applications (Jayaraman et al. 2025). Traditionally, inverters were limited to two voltage levels (+V and –V), regulated through Pulse Width Modulation (PWM) techniques (Esmaeili and Koofigar 2024). However, this methodology is prone to issues such as prominent harmonic distortion, electromagnetic interference (EMI), and dv/dt stress (Das et al. 2024). The foremost concern is the high Total Harmonic Distortion (THD) and the need to reduce semiconductor-related switches (Memon et al. 2024) in mid- and high-voltage grids (2.3, 3.3, 4.16, or 6.9 kV).

To address these limitations, the concept of multilevel inverters (MLIs) was introduced. By utilizing multiple voltage levels (Dewangan et al. 2023), MLIs not only effectively diminish harmonic distortion (Liu et al. 2023) but also generate a smooth sinusoidal output waveform and distribute voltage stress more efficiently across power electronic switches (Chattejee, Chakraborty, and Dalapati 2023). Therefore, these devices have become increasingly important in industrial applications such as static VAR compensators, renewable energy systems, and motor drives.

Over the past few years, numerous MLI topologies (Khasim and Dhanamjayulu 2022) have been developed, including Cascaded H-Bridge (CHB-MLI), Flying Capacitor (FC-MLI), and Diode-Clamped (DC-MLI) configurations (Thakre et al. 2022). Each of these utilizes independent DC sources, contributing to operational flexibility. With multiple voltage levels achieved through the integration of power switches, capacitors, and diodes (Salem et al. 2022), these topologies generate stepped waveforms (Guo et al. 2022).

In the evolution of MLI technology, three-level designs, characterized by voltage levels (0, +Vdc, and −Vdc), have been a significant step forward. MLIs facilitate the creation of a refined staircase waveform (Zhu et al. 2022), improving power quality by incorporating more voltage levels. This advancement helps reduce THD and dv/dt stress (Choudhury et al. 2021), thereby enhancing reliability and efficiency. However, as voltage levels increase, challenges such as switching complexity and voltage imbalance arise (Iqbal et al. 2021), requiring advanced control and modulation techniques (Perez et al. 2021).

Cascaded hybrid MLIs with isolated DC sources are among the most prominent topologies due to their ability to operate without capacitors and diode clamping (Marquez et al. n.d.). Increasing

the number of H-bridges enhances voltage levels and waveform quality but also increases control complexity and the number of required switches (Ramesh et al. 2020).

The novelty of the proposed three-phase 25-level inverter lies in its modular nested architecture, which differs from conventional Cascaded H-Bridge (CHB) and Neutral Point Clamped (NPC) configurations. Unlike existing reduced switch-count MLIs, which often suffer from increased voltage stress (Ahmed et al. 2020) or complex DC source balancing, the proposed topology utilizes a hybrid level-generation unit integrated at the phase-leg level (Prem et al. 2020). This design employs unequal DC sources and a sub-multilevel cell structure to produce 25 levels with approximately 40% fewer active switches than conventional CHB topologies. The shared-bus arrangement across three phases eliminates the need for redundant isolation transformers and excessive clamping diodes (Siddique et al. 2019).

Although this topology offers advantages such as reduced components, elimination of clamping diodes and voltage-balancing capacitors, and support for soft-switching techniques (Lee, Kim, and Lee 2020), it still requires separate DC sources, which may limit certain applications (Monopoli et al. 2019). The lower THD in the three-phase configuration is mainly due to the cancellation of triplen harmonics (3rd, 9th, 15th, etc.). In a balanced three-phase system, these harmonics are in phase and cancel out in line-to-line voltages, resulting in a cleaner waveform for PMSM applications.

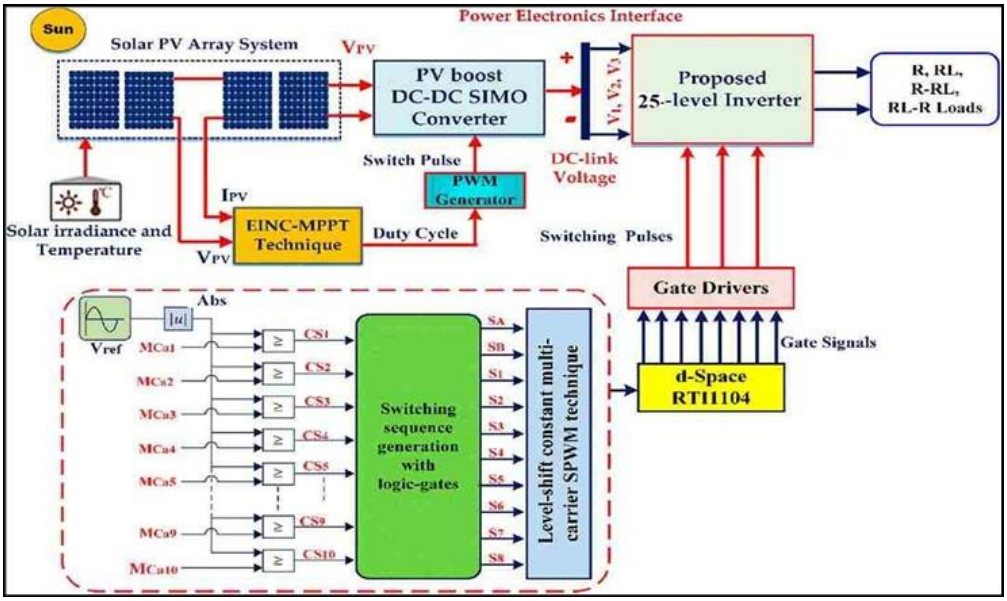

Figure 1. Schematic Exemplary of HEV

II. RESEARCH METHOD

A. Hybrid Electric Vehicles

Figure 1 illustrates the schematic exemplary of HEV. This system comprises four key

components, electric motor, a generator, a battery management system, and DC/DC converter topology. Each component plays a vivacious role in overall functionality. It effortlessly manages and coordinates the driving forces generated via ICE, electric motor and generator by leveraging a planetary gear system. To ensure smooth transitions, optimizing vehicle performance between propulsion sources and improving overall efficiency, this collaboration is crucial.

A 57 kW gasoline engine operating at 6000 RPM, the ICE subsystem configuration designed for high-performance output. The engine maintains stability by regulating speed and preventing overshooting, equipped with a speed governor. Along with, Vehicle Dynamic subsystem integrates all mechanical components such as, chassis, suspension, wheels, and steering system. All of these play a key role in vehicle handling, stability and driving comfort. Additional essential subsystem is Energy Management Subsystem (EMS), adapts to dynamic driving conditions and energy demands. This is responsible for producing precise reference signals to coordinate the motor drive, generator and ICE operation. Also EMS subsystem monitors and optimizes energy flow in order to improving both efficiency and longevity of the vehicle's electrical systems.

The architectural design of EVs offering a significant opportunity for encroachments via unified integration of key components which enhance efficiency and overall performance. The chief parts of the system are batteries, motors and inverters, which transform DC from the battery into AC to drive the motor. Furthermore, in gathering and processing data, optimizing vehicle performance and safety sensors play a decisive role in the system. Moreover, supplementary systems such as ventilation heating and air conditioning contribute to passenger comfort, increasing the overall driving experience. In this modeling, the design and integration of key components in electric vehicles, choice between a 400 Volt and 800 Volt battery systems plays a crucial role. By carefully selecting and strategically arranging these components, efficient EVs can align with sustainability intentions and evolving consumer demands. Here two conversions takes place viz. DC/DC and DC/AC.

B. Dynamic Modeling and Control of DC/DC & DC/AC Converter Configuration

1. DC/DC Modeling

Transformerless inverters need a voltage boost stage when processing power from low-voltage sources to keep the DC bus voltage at a suitable level for transferring power to the load or grid. This challenge can be addressed with a configuration where the necessary voltage step-up is achieved using a 2-stage converter, which contains a DC/DC boost converter followed by a voltage source inverter (VSI). Numerous articles discuss various

DC/DC converters suitable for renewable energy applications, with most topologies exhibiting voltage source features in their outputs. While this feature can lessen the output voltage ripple when feeding linear loads, it needs an additional inductor for claims where the converter shoots up current into the utility grid. Moreover, the shoot up current cannot be pre-controlled by the DC/DC converter, causing the DC/AC stage that links the converter to the grid to switch at high frequencies, thereby growing overall system losses.

Thus, the DC/DC boost-buck converter emerges as a robust power converter for these applications. This topology combines the boost and buck structures into a non-isolated, bidirectional, step-up/step-down DC-DC converter with high power density and continuous I/P and O/P currents. Additionally, it is a multipurpose converter suitable for various applications including PV systems, high-efficiency wireless power transfer AC power generation, PF correction and thermoelectric generators. Furthermore, it can be modified for multilevel and 3-phase applications. The schematic of the DC-DC configuration for HEV is depicted in Figure 2.

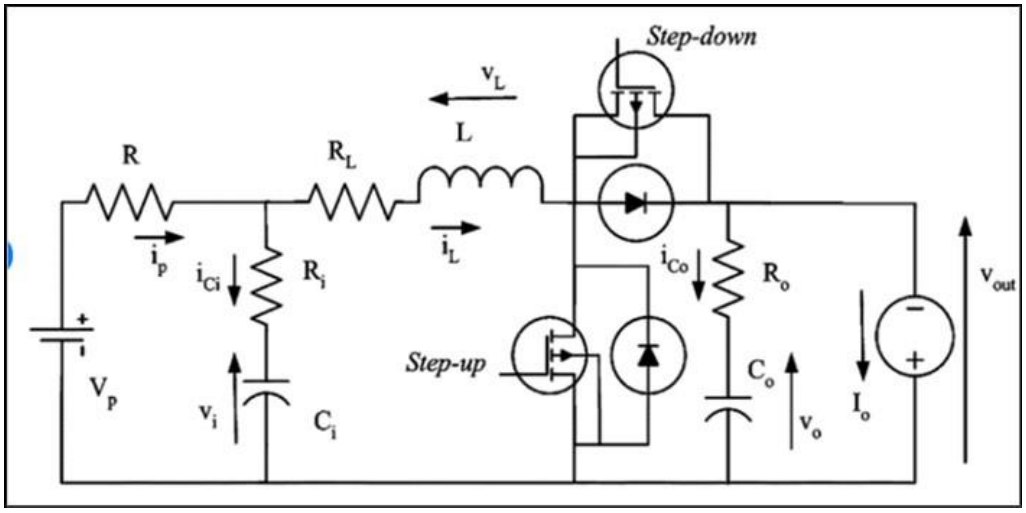

Figure 2. DC-DC Configurations

The characteristics of the DC-DC power converter at no losses (ideal case) can be expressed by Equation (1) and Equation (2).

$$w_{dc\_in} = v_{in}.i_{in} \tag{1}$$

$$w_{dc\_out} = v_{out}.i_{out} \tag{2}$$

The power at the intermediate DC link is defined by Equation (3).

$$w_{dc\_out}^{dc-dc} = w_{in}^{invt} + w_{loss} \tag{3}$$

Where,

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$w_{dc_{out}}^{dc-dc}$ = Power output of DC - DC power converter

w_{in}^{invt} = Inverter input of DC-DC power converter

w_{loss} = Power loss at DC-DC power converter

By considering dynamic storage, the system behavior is captured in Equation (4).

$$c_{link} \cdot v_{dc} \frac{dv_{dc}}{dt} = w_{dc\_out}^{dc-dc} - w_{in}^{invt} \quad (4)$$

The converter output power is calculated using Equation (5).

$$w_{dc\_out} = \eta_{dc-dc} \cdot w_{dc\_in} = v_{dc} \cdot i_{dc} \quad (5)$$

Where,

c_{link} = capacitor link

v_{dc} = DC voltage

i_{dc} = DC current

Figure 3 depicts the input voltage waveform of DC/DC converter, whereas Figure 4, and Figure 5 depicts its out-put voltage and current waveform respectively.

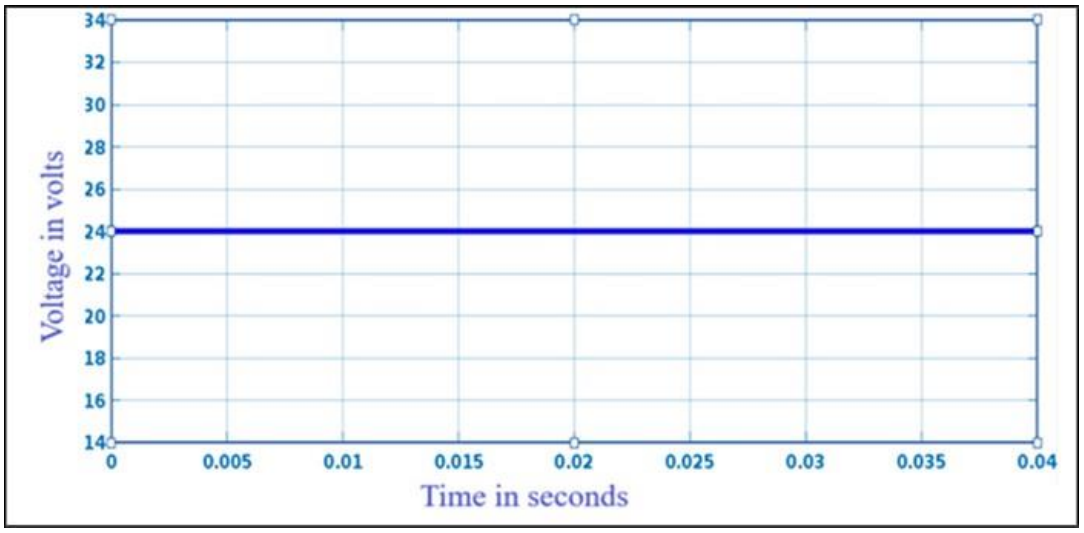

Figure 3 Input Voltage Waveform of DC/DC Converter

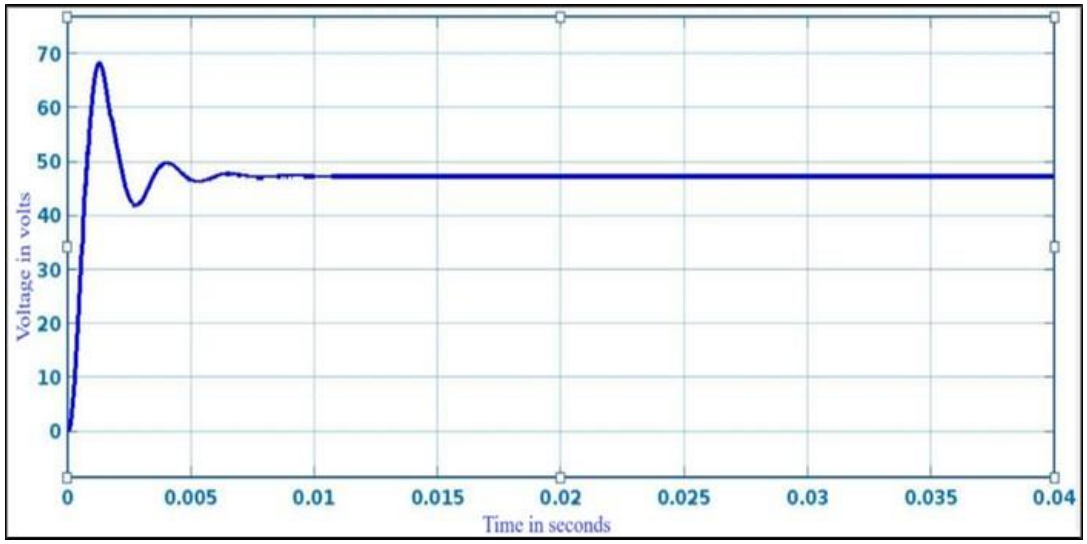

Figure 4. Output Voltage Waveform of DC/DC Converter

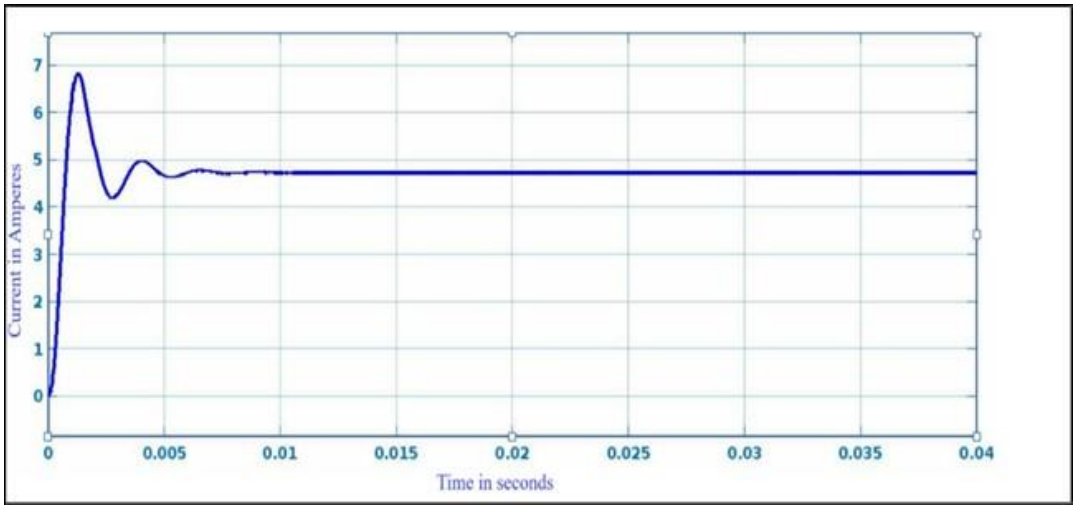

Figure 5. Output Current Waveform of DC-DC Converter

2. DC/AC Modeling

Modern PE heavily relies on DC/AC converters, as they enable the transformation of DC sources into AC essential for most electrical applications. These converters play a critical role in several domains, including motor drives; uninterruptible power supplies (UPS), EVs and renewable energy systems. In this converters including both 1-ph. and 3-ph. inverters along with progressive modulation technique. It also covers the key components such as circuit topologies and operational modes. There are two key types of inverters-viz. Voltage-Sourced Inverters (VSI) and Current-Sourced Inverters (CSI). VSIs generate the desired AC output voltage waveform while upholding a constant input DC voltage. Whereas CSIs produce the desired AC out- put current waveform using a persistent input current. Since both VSI and CSI are duals, their functionalities can be understood by comparing their respective voltage

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and current dualities. Figure 6 below depicts the operating model of inverter configurations for electric vehicles.

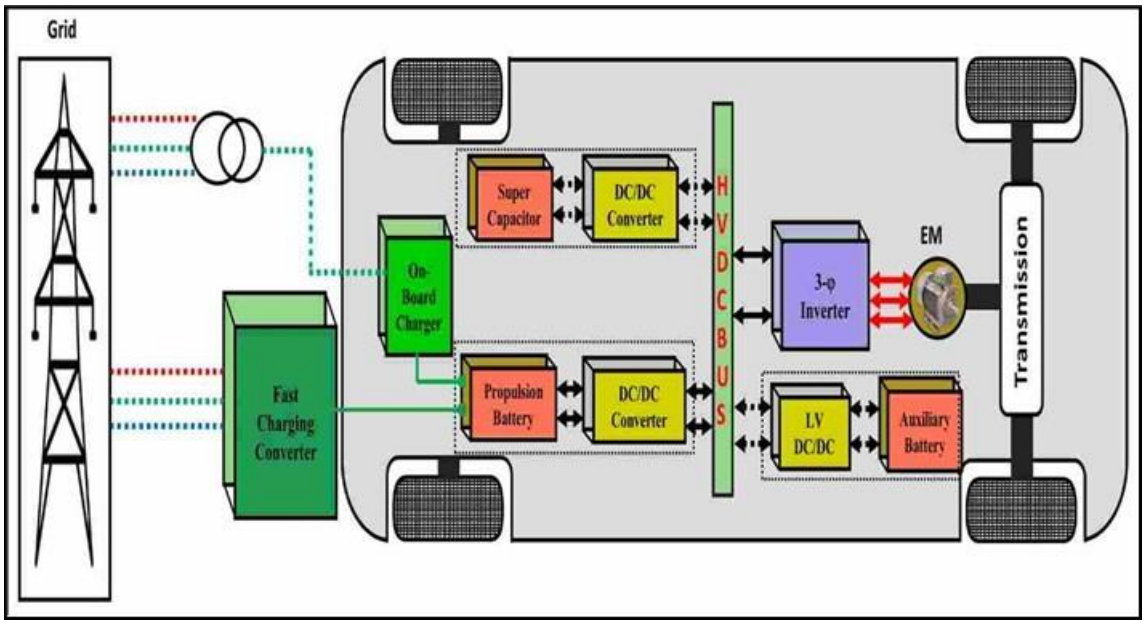

Figure 6. EV Configuration with Inverter Topology

The input DC power to the inverter within the DC-AC converter stage is given by Equation (6).

$$w_{in}^{invt} = v_{dc} . i_{dc} \tag{6}$$

Where,

w_{in}^{invt} = Inverter input (DC-AC conevrter)

For a balanced three-phase system, the output AC power in the dq reference frame is expressed in Equation (7).

$$w_{ac} = \frac{3}{2}(v_d i_d + v_q i_q) \tag{7}$$

Where,

w_{ac} = AC power output
v_d = direct axis voltage
i_d = direct axis current
v_q = quadrature axis voltage
i_q = quadrature axis current

Furthermore, to determine the converter output power for a 3-phase inverter, the fundamental component of the line-to-line (L-to-L) output voltage and power relationship

is given by Equation (8).

$$w_{ac\_out} = \eta_{dc-ac}.w_{invt\_in} = \sqrt{3}v_{LL}.i_L\cos(\phi) \quad (8)$$

Where

ηdc–ac = Inverter efficiency
vLL = Line-to-line voltage
iL = Line current
cos(φ) = Power factor

By combining the previous stages, the total power flow of the system, often referred to as the Collaborative System Equation, is formulated in Equation (9).

$$w_{total} = \eta_{dc-ac}.\eta_{dc-ac}.w_{dc\_in} = \eta_{in}.w_{dc\_in} \quad (9)$$

This is the core collaborative equation, showing how input DC power is converted efficiently into motor- driving AC power. For an HEV, the DC/DC converter and DC/AC converter (inverter) work together to manage and convert power from the battery (source) to drive the AC load and vice versa during regenerative braking.

Finally, the relationship that defines the intermediate high-voltage DC for the inverter is provided in Equation (10).

$$\eta_{dc-ac} = efficiency\ of\ the\ DC/AC\ coverter \quad (10)$$

This provides the intermediate high-voltage DC for the inverter.

C. Phase Disposition (PD) in Multi-Carrier PWM

Phase Disposition (PD) is a widely used multi-carrier Pulse Width Modulation (PWM) technique designed for controlling MLIs. Its primary objective is to generate a smooth AC output waveform while significantly reducing harmonic distortion. In PD-PWM, multiple high-frequency triangular carrier signals are employed. At the starting all of these remain coordinated and maintaining alignment throughout the modulation process at the same point. A low-frequency sine wave serves the reference signal, which is unceasingly compared with the carrier signals.

The switches of the inverter are triggered based on whether the reference falls below each carrier or signal surpasses. Forming an output waveform that closely resembles a pure sine wave, this progression results in the generation of multiple voltage levels. Synchronization of all carriers ensures a more balanced waveform with minimal harmonic distortion, improves waveform smoothness and symmetry for more efficient power conversion (improved output

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voltage quality) are key advantages of this technique. PD-PWM is widely adopted in industrial applications and easier to implement when comparing with alternative PWM techniques such as Phase-Opposition Disposition (POD) and Alternative-Phase Opposition Disposition (APOD). Figure 7 depicts the Phase-Disposition (PD) in Multi-Carrier PWM, used for generating gate pulses for the proposed 25-level MLI topology.

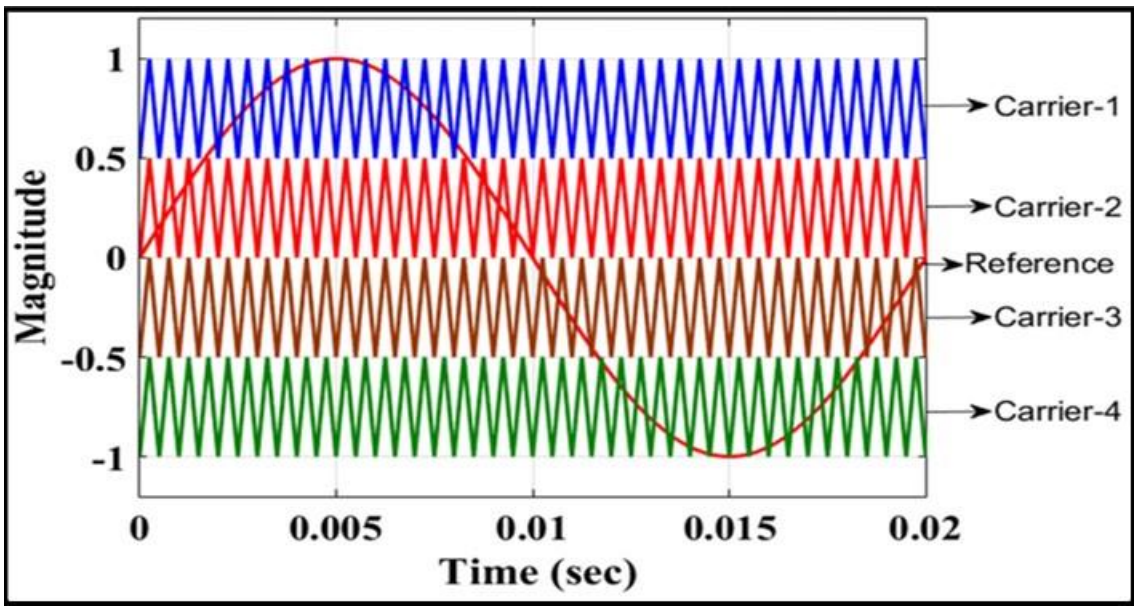

Figure 7. Phase-Disposition in Multi-Carrier PWM

III. RESULT

A. Single Phase 25- Level Mli Topology

Single phase 25-level MLI configuration utilizes four distinct, unequal DC sources and 12 switches to achieve output voltage ranging from +12 Vdc to -12 Vdc successfully. Figure 8 represents the MATLAB/Simulink model of proposed 1-phase 25-level MLI. This configuration significantly optimizes efficiency by minimizing DC sources by 67% and reducing the number of switches by 75%. Table 1 summarizes the necessary switching patterns for generating the desired 25-level output voltage. To mitigate THD and further enhance the performance, various pulse-width modulation (PWM) techniques being employed in multilayer inverters. Numerous multicarrier PWM methods are available to improve waveform quality. This study specifically implements a multicarrier-PWM (MCPWM) strategy with PD, effectively reducing THD in both output voltage and current.

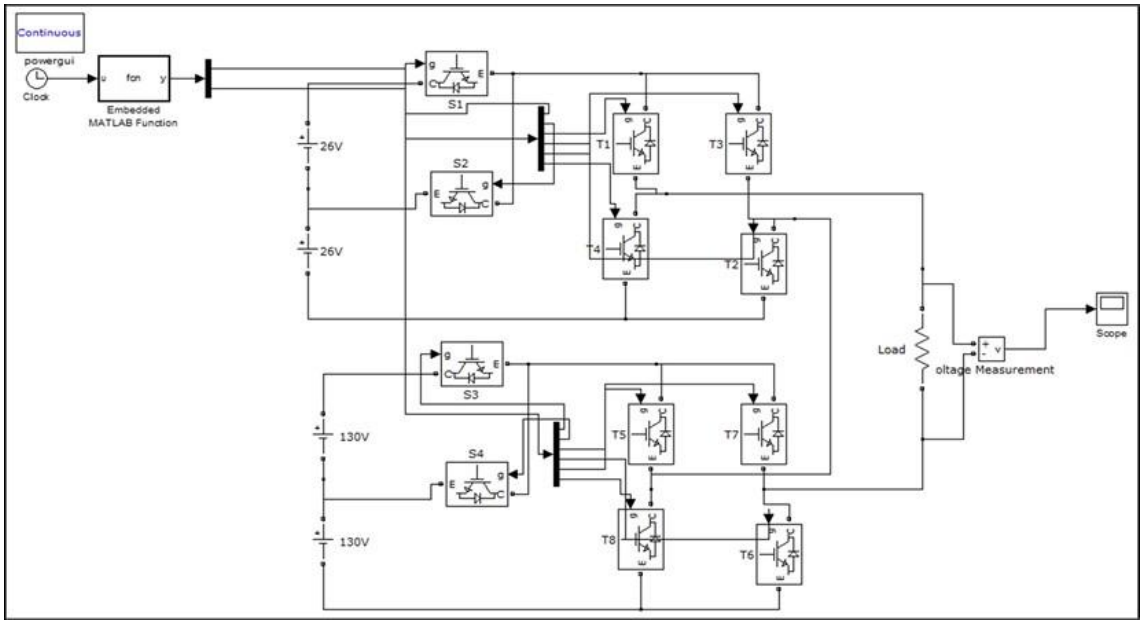

Figure 8. Single Phase 25 Level Inverter Using Sub-Multilevel Cells

Growing interest in MLIs for medium-voltage industrial applications in recent times. As the number of levels increases, the complexity of the power and control circuits in typical MLIs also tends to rise, owing to the increased number of driving circuits and other constituents involved. This increase in discrete components may impact system reliability. To address these challenges, various MLI topologies have been thoughtfully developed to enhance component efficiency while simultaneously improving the output voltage waveform. Recent research efforts in this area have explored techniques for fine-tuning triggering angles, which can aid in minimizing the generated harmonics, during the operation as well as reduce the overall number of required switches. For a typical cascaded-MLI circuit, the calculation of switching devices and DC sources is determined by Equation (11) and Equation (12).

$$Switch\ count\ =\ 2(Level\ -\ 1) \tag{11}$$

$$DC\ Source\ count\ =\ (Level\ -\ 1)/2 \tag{12}$$

For a single-phase 25-level inverter, the switching table typically lists the states of switches corresponding to each voltage level. Since the same switching logic is applied to the other two phases with a 120° phase shift, the table remains consistent across phases, with appropriate phase offsets.

In the recommended configuration, the total number of switching devices and DC sources for the entire system are chosen as follows, represented by Equation (13) and Equation (14).

$$Switch\ count\ =\ (Level\ -\ 1)/2 \tag{13}$$

$$DC\ Source\ count\ =\ (Level\ -\ 1)/6 \tag{14}$$

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Furthermore, the number of H-bridge cells per phase required to achieve the desired levels is given by Equation (15).

$$m = 2N + 1 \quad (15)$$

Where,

m = the number of voltage level

N = the number of H-bridge cells per phase For 25 levels, N = 12

The total output voltage generated by the cascaded configuration is expressed in Equation (16).

$$v_{out}(t) = \sum_{i=1}^{12} v_i(t) \quad (16)$$

Where,

$v_i(t) \in \{-v_{dc}, 0, +v_{dc}\}$

It provides voltage levels ranging from -12 V_{dc} to +12 V_{dc}, resulting in 25 discrete steps: -12 V_{dc}, -11 V_{dc}, -10 V_{dc}, ..., 0, ..., +10 V_{dc}, +11 V_{dc}, +12 V_{dc}.To analyze the harmonic content, the total output voltage in Fourier series form is formulated in Equation (17).

$$v_{out}(\omega t) = \sum_{n=1,3.5\ldots}^{\infty} \left(\frac{4v_{dc}}{n\pi} \sum_{k=1}^{12} \cos(n\theta_k)\right)(\sin(\omega t)) \quad (17)$$

Where

n = odd harmonic number

θ_k = switching angle of k^{th} cell (for positive half cycle)

By solving this to eliminate lower order harmonic like 5^{th}, 7^{th}, 9^{th} , 11^{th} etc. by maintaining the fundamental. Finally, the modulation index (M_i), which relates the reference voltage to the maximum obtainable voltage, is defined by Equation (18).

$$m_a = \frac{v_{ref}}{12v_{dc}} \quad (18)$$

Where,

$v$ref = Desired fundamental voltage peak of the out-put fundamental component.

The proposed design thoughtfully incorporates four distinct DC voltage sources (130. 130, 26 & 26 V), utilizing a total of 12 switches to achieve an impressive 25-level output voltage range from +12 V_{dc} to - 12V_{dc}. This innovative configuration offers significant benefits, including a 75% reduction in the number of switches and a 67% decrease in the number of

DC sources. The arrangement of the DC voltage sources in thoughtfully organized in a ratio of 1: 1.5: 5 V_{dc}. For further clarification, Table.1 provides the switching- patterns of MLI needed to attain the desired 25-level output voltage. Figure. 9 depicts a comprehensive current route diagram for the inverter system's various modes operation.

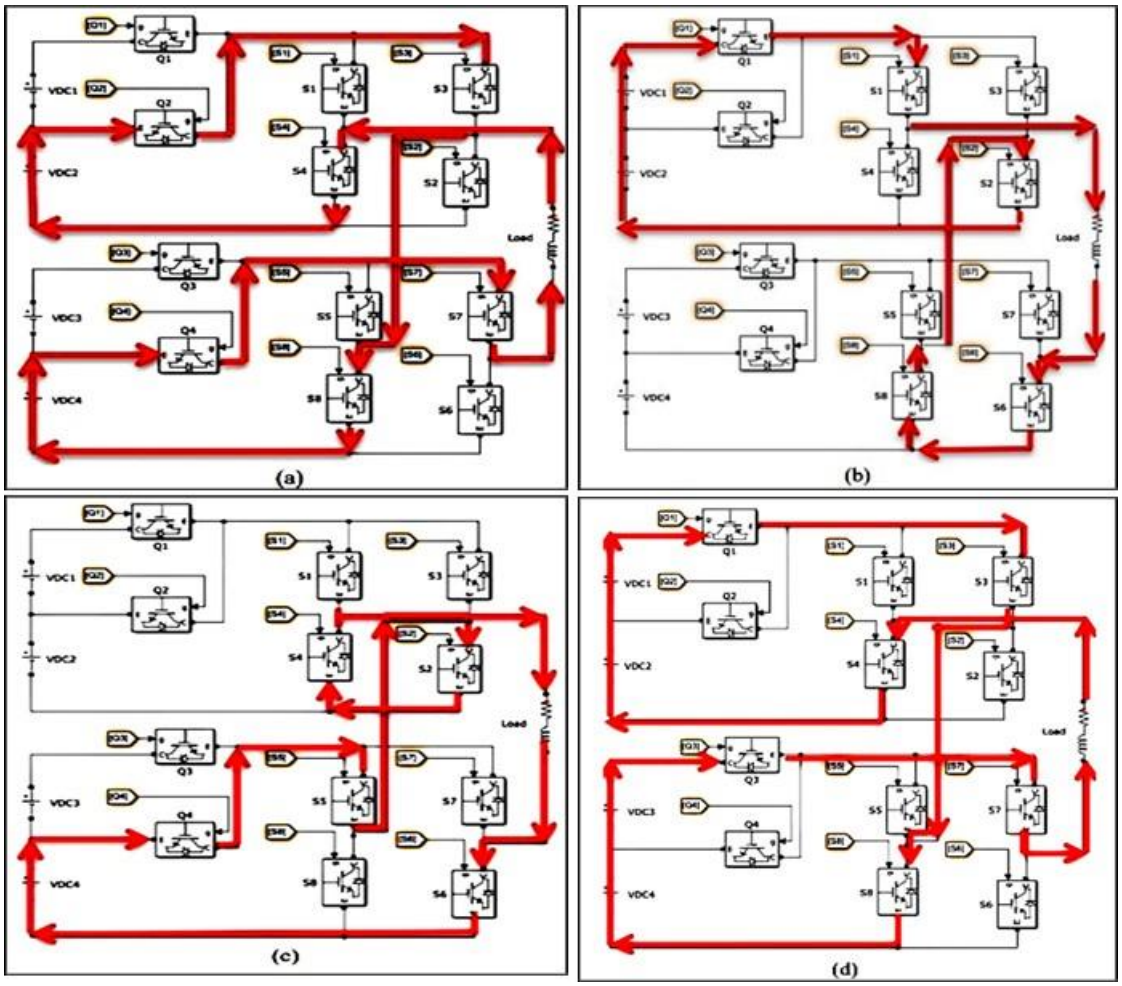

Figure 9. Current Path Diagram in Various Operating Modes at Output Voltage of a). +12 V_{dc}, b). – 6 V_{dc}, c). +5 V_{dc},, d). -12 V_{dc}.

Figure 9 (a) depicts, the current route used to obtain an output voltage of +12 V_{dc}, which is especially important for specific applications. Figure. 9 (b) depicts the current route required to provide an out-put of +6 V_{dc}, a configuration that is frequently used in power supply applications that need a negative voltage reference. Figure. 9 (c) depicts the current route for producing a +5 V_{dc} output voltage, which is commonly used standard for low-voltage electronic equipment. Finally, figure 9 (d) displays the current route required to obtain an out-put voltage of-12V_{dc}, which is frequently used in analog circuits and other specialized electronic applications. By assuming a symmetric waveform with 25 levels, the calculation for the RMS voltage (Vrms) and its relationship to each voltage step is given by Equation (19) and

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Equation (20).

$$V_{RMS} = \sqrt{\frac{1}{T}\left(\int_0^T V_0^2(t)dt\right)} \quad (19)$$

$$V_{RMS} \approx \sqrt{\frac{1}{T}\left(\sum_{k=1}^{n}(V_k^2.\Delta t_k)\right)} \quad (20)$$

Where,

V_k = Voltage at each level

Δt_k = Duration of level

Table 1 presents the switching states for the proposed 25-level MLI topology, and Figure 10, Figure 11 depicts the out-put voltage waveform and its FFT analysis for 1-phase 25-level MLI respectively. To improve the performance and stability, numerous PWM approaches were carefully incorporated with multilayer inverters, resulting in a considerable reduction in total THD. This decrease is critical for ensuring the quality of power transmission and limiting potential interference with other electronics. Furthermore, it was tested numerous multicarrier PWM systems for efficacy in a variety of settings

Table 1. Switching States of 25-Level Output Voltage

Conducting switches: 1=ON, 0=OFF													
Level	**Q1**	**Q2**	**Q3**	**Q4**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**	**V_{0ut}**
1	1	0	1	0	1	1	0	0	1	1	0	0	$12V_{dc}$
2	0	1	1	0	1	1	0	0	1	1	0	0	$11V_{dc}$
3	0	0	1	0	0	1	0	1	1	1	0	0	$10V_{dc}$
4	0	1	1	0	0	0	1	1	1	1	0	0	$9V_{dc}$
5	1	0	1	0	0	0	1	1	1	1	0	0	$8V_{dc}$
6	1	0	0	1	1	1	0	0	1	1	0	0	$7V_{dc}$
7	0	1	0	1	1	1	0	0	1	1	0	0	$6V_{dc}$
8	0	0	0	1	0	1	0	1	1	1	0	0	$5V_{dc}$
9	0	1	0	1	0	0	1	1	1	1	0	0	$4V_{dc}$
10	1	0	0	1	0	0	1	1	1	1	0	0	$3V_{dc}$
11	1	0	0	0	1	1	0	0	0	1	0	1	$2V_{dc}$
12	0	1	0	0	1	1	0	0	0	1	0	1	$1V_{dc}$
13	0	0	0	0	1	1	1	0	1	0	1	0	0
14	0	1	0	0	0	0	1	1	1	0	1	0	$-1V_{dc}$
15	1	0	0	0	0	0	1	1	1	0	1	0	$-2V_{dc}$
16	1	0	0	1	1	1	0	0	0	0	1	1	$-3V_{dc}$
17	0	1	0	1	1	1	0	0	0	0	1	1	$-4V_{dc}$
18	0	0	0	1	1	0	1	0	0	0	1	1	$-5V_{dc}$
19	0	1	0	1	0	0	1	1	0	0	1	1	$-6V_{dc}$
20	1	0	0	1	0	0	1	1	0	0	1	1	$-7V_{dc}$
21	1	0	1	0	1	1	0	0	0	0	1	1	$-8V_{dc}$
22	0	1	1	0	1	1	0	0	0	0	1	1	$-9V_{dc}$
23	0	0	1	0	1	0	1	0	0	0	1	1	$-10V_{dc}$
24	0	1	1	0	0	0	1	1	0	0	1	1	$-11V_{dc}$

25	1	0	1	0	0	0	1	1	0	0	1	1	$-12V_{dc}$

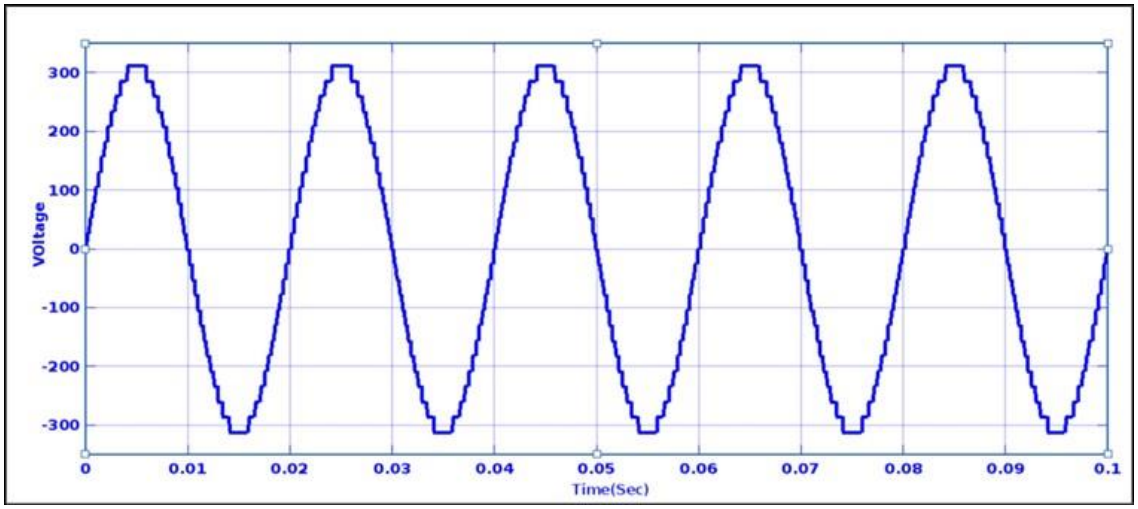

Figure 10. Output Voltage Waveform of 1-Phase 25-Level MLI

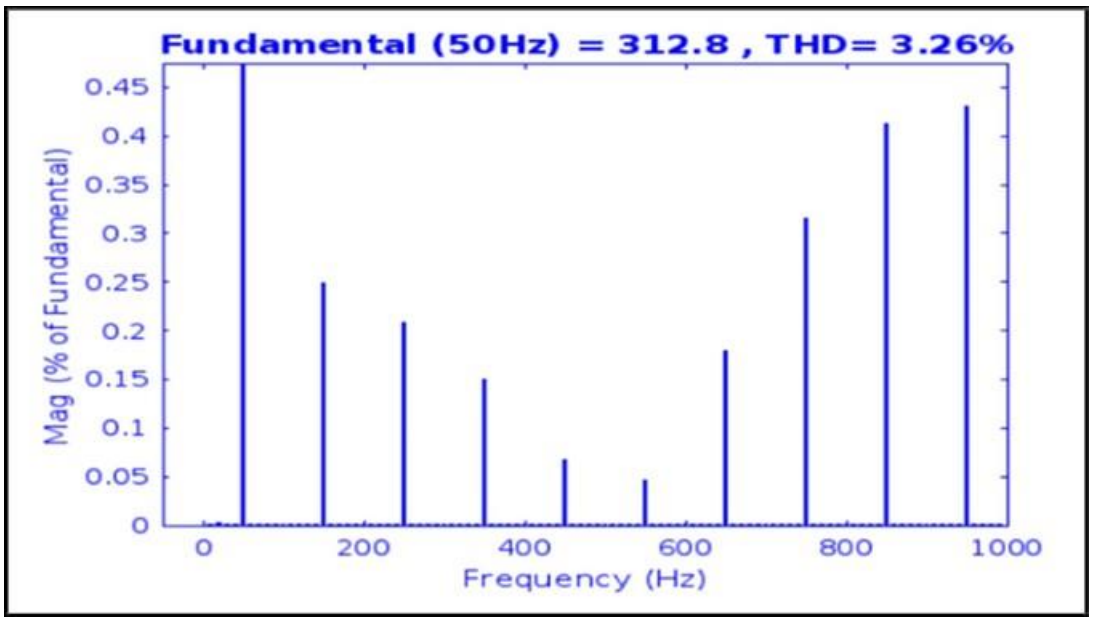

Figure 11. FFT Analysis for 1-phase voltage

In this work, it was selected to use a multicarrier PWM (MC-PWM) technique based on phase disposition (PD) methodology. To optimize waveform morphologies and achieve lower THD levels in both output voltage current, this approach is especially designed resulting in improved overall system performance and efficiency

B. Proposed 3-Phase 25- Level MLI Configuration

The 3- phase 25-level MLI is a type of power converter used in HEVs to reduce THD improve the efficiency and enhance power quality. These inverters are designed to provide higher voltage levels with reduced switching losses making them ideal for EV applications.

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Figure 12 represents the Mat lab/Simulink model of proposed three phase 25-level MLI. With this converter, the output voltage of the single phase 25-level MLI wave form as shown in the Figure 13.

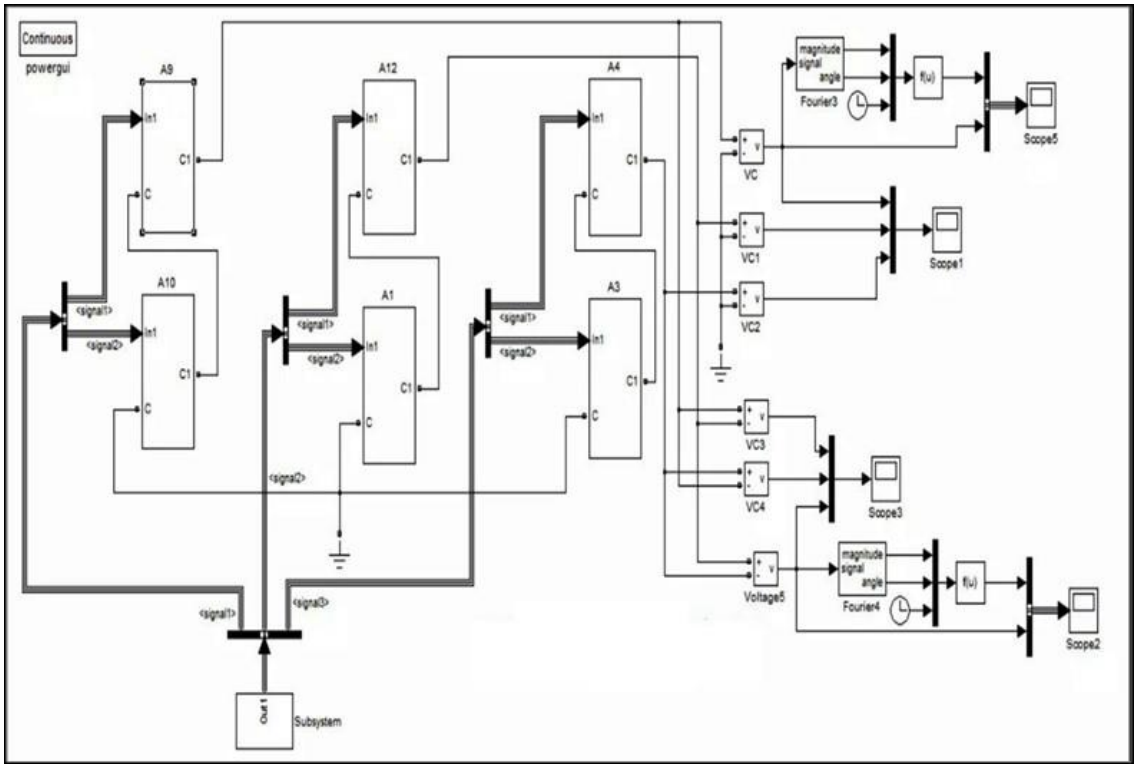

Figure 12. Mat lab/Simulink Model of Proposed Three Phase 25-Level MLI

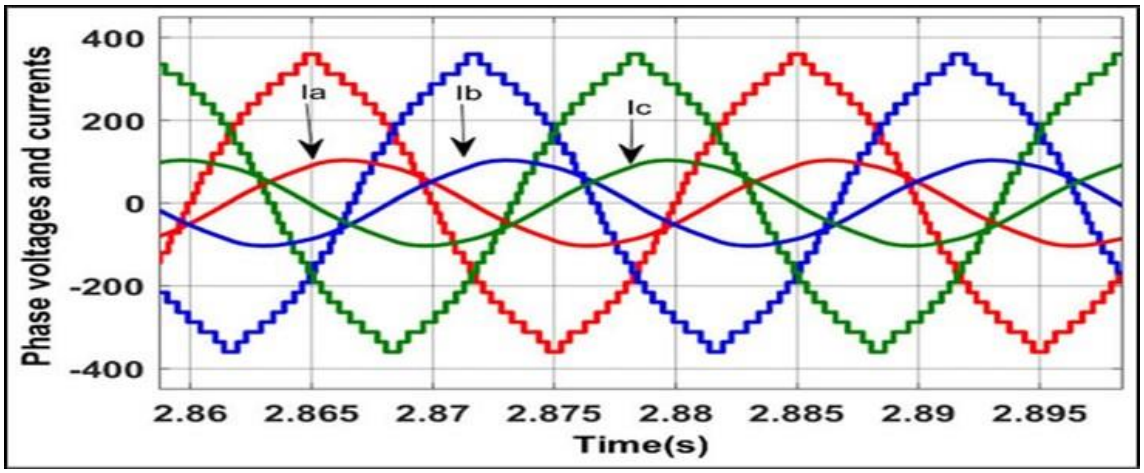

Figure 13. Output Waveforms of Three Phase MLI

FFT analysis is an effective method for decomposing signals into their frequency components and is applicable to both 1-phase and 3-phase voltage signals. When it comes to three-phase signals, the analysis considers three distinct voltage waveforms.

This approach enables the identification of phase imbalances and harmonic distortion in the

system, contributing to a more comprehensive understanding of its performance. Figure.14 depicts the FFT analysis for 3-phase output voltage of proposed 25-level MLI. The comparative analysis between proposed 1-ph. and 3-ph. 25-level MLI topologies is given in the Table 2.

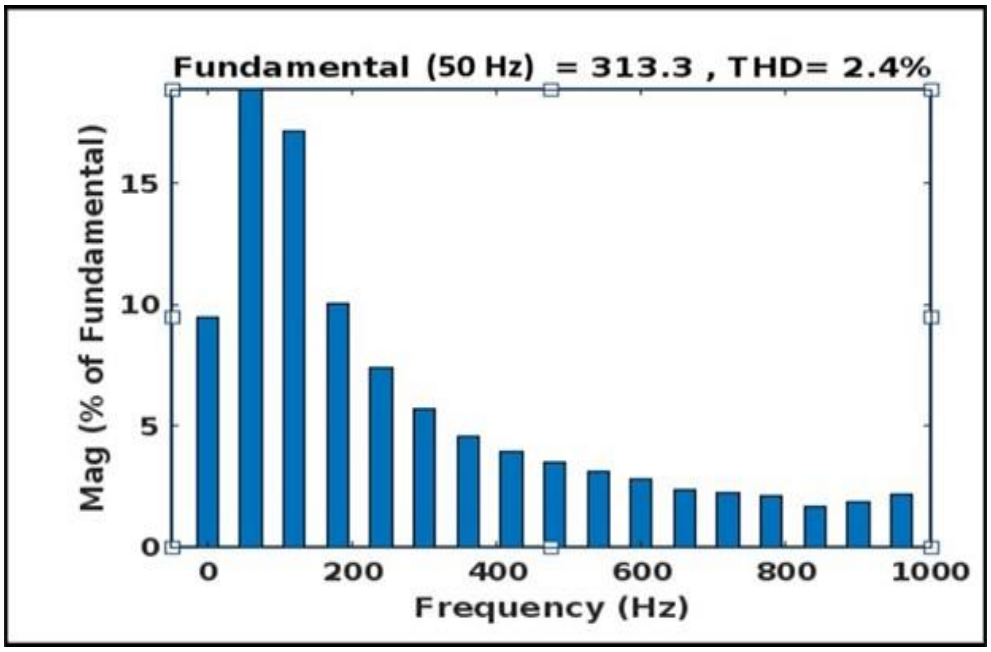

Figure 14. FFT Analysis for 3-Phase Voltage

Table 2. Comparative Analysis

Parameter	Single-Phase 25-Level	Three-Phase 25-Level	Technical Driver
Maximum voltage	312.8V	313.3V	Approximately equal
frequency	Fundamental 50 Hz	Fundamental 50 Hz	Same frequency
THD (%)	3.26 %	2.40 %	Cancellation of triplen harmonics.
Torque Ripple	Pronounced	Minimal	Constant instantaneous power flow.
DC Bus Stress	High (Pulsating)	Low (Balanced)	Phase-offset current demands.
Filter Size	Large	Compact / Optional	Waveform closer to ideal sine.

IV. CONCLUSION AND RECOMMENDATION

Hybrid electric vehicles (HEVs) are emerging as a significant technology for both present and future generations. These vehicles are complex dynamic systems, with 3-phase inverters being utilized for high- power applications. When engaging a voltage source inverter functioning in 120o conduction mode, harmonic losses and copper winding are minimized, ensuring accurate output waveforms for rotor speed, rotor angle and electromagnetic torque in both open loop and closed loop configurations. Simulation results obtained using the Mat lab/Simulink environment, demonstrate the effectiveness of this study. To summarize, the proposed 3-phase 25-level

integrated inverter configuration offers a highly efficient and forward-thinking solution for hybrid electric vehicles (HEVs).

By carefully optimizing the number of switching-components and DC-sources, this design effectively minimizes system complexity while maintaining superior out-put voltage quality with reduced THD. In this study, the proposed system has achieved a low THD of 2.4%. These results were obtained under consistent operating conditions, including the same modulation index, switching frequency, and load parameters, to avoid potential ambiguity in the comparison and valid within the assumptions of the MATLAB/Simulink modelling environment, with experimental validation deferred to future work. Furthermore, by using advanced multicarrier PWM techniques refines performance, ensuring seamless transitions across voltage levels. Moving forward, future studies could focus on advancing modulation strategies and exploring system-wide integration to improve scalability and adaptation across various electric vehicle platforms

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